memory hierarchy. [executes instructions from the memory hierarchy and a replay handler is loaded into the memory hierarchy and the processor executes the replay handler for replaying at least one execution.]

3. (Amended) The system of claim 1 wherein the [the] replay handler is loaded into the memory hierarchy in response to a signal.

4. (Amended) The system of claim 1 wherein the replay handler includes the plurality of instructions. [at least on execution.]

5. (Amended) The system of claim 1 wherein the replay handler loads the [at least one execution] plurality of instructions into the memory hierarchy from an external device.

6. (Amended) A system for replaying executions comprising:

a storage element;

a memory hierarchy coupled to the storage element;

a system bus coupled to the memory hierarchy; and

a processor coupled to the system bus, wherein the processor executes instructions from the memory hierarchy and wherein on a break, the processor reaches a steady state, transfers original code of the memory hierarchy to the storage element, loads a replay handler into the memory hierarchy and the processor executes the replay handler to repeatedly replay at least one execution[.] to test for proper operation of the processor, wherein the at least one execution includes a plurality of instructions.

7. (Amended) The system of claim 6 wherein the original code is loaded into the memory hierarchy after the at least one execution has been repeatedly replayed.

10. (Amended) A system comprising:

a memory hierarchy;

a processor coupled to the memory hierarchy wherein the processor executes instructions from the memory hierarchy;

a port coupled to the processor and memory hierarchy;

a host system coupled to the port; and

wherein the host system generates a replay handler, generates at least one execution to be repeatedly replayed by the processor when executing the replay handler, and generates a signal to the processor to cause the processor to load the replay handler into the memory hierarchy and repeatedly replay [for replaying] the at least one execution.

17. (Amended) A method for replaying executions comprising:

interrupting normal processor execution;

loading a replay/restart kernel;

repeatedly replaying at least one execution to test for proper operation of a processor, wherein the at least one execution includes a plurality of processor instructions; and

resuming normal executions.

20. (Amended) A method comprising:

interrupting processes executing on a processor;

storing minimal state information sufficient to later resume the interrupted processes;

storing original code of an instruction cache;

loading a replay handler into the instruction cache;

branching execution of the processor to the replay handler;

replaying a system execution a number of times from a starting point to a stopping point while monitoring state information to test for proper operation of the processor;

loading the original code into the instruction cache; and

resuming interrupted processes utilizing the minimal state information.

23. (Amended) A computer readable medium containing computer instructions for instructing a processor to perform a method of:

generating at least one execution that includes a plurality of processor instructions;

interrupting normal processing;

loading a replay handler;

repeatedly replaying the at least one execution to test for proper operation of the processor;

accessing state information;

storing state information; and

resuming normal processing.

REMARKS

Applicant has carefully reviewed and considered the Office Action mailed on August 14, 2002, and the references cited therewith.

Claims 1, 3, 4-6, 7, 10, 17, 20, and 23 are amended, and no claims are canceled or added; as a result, claims 1-23 are now pending in this application.

Claim Objections

Claims 3 and 4 were objected to because claim 3 included "the the" instead of "the", and claim 4 included "on" instead of "one". Applicant has amended claims 3 and 4 to overcome this rejection. These amendments have not been made for reasons of patentability.

Rejections Under 35 U.S.C.§103

Claims 1-4 and 17-19 were rejected under 35 U.S.C.§103(a) as being unpatentable over Mealey et al. (U.S. Patent No. 5,963,737) in view of Zumkehr et al. (U.S. Patent No. 6,247,118 B1). Independent claims 1 and 17 have been amended. Applicant respectfully submits that these claims, as amended, define over the references of record. Applicant further submits that dependent claims 2-4, 18, and 19 also define over the references of record. Accordingly, applicant respectfully submits that claims 1-4 and 17-19 are in condition for allowance.